NEW DATA UPDATE 9

NATIONAL SEMICONDUCTOR CORPORATION

MAY 1983

NEW DATA UPDATE 9

NATIONAL SEMICONDUCTOR CORPORATION

The New Data Update 9 is provided by National Semiconductor in order to keep you abreast of the latest products available. This special issue features the first pages of data sheets published February 1983 through April 1983 (1 quarter). Two alphanumerical indexes, one by device number and one by device function, serve as guides to the contents of this Update. A third index provides a listing of new application notes and briefs. These indexes/tables of contents are located in the front of the book. One additional index serves as an ordering guide for all other application notes and briefs which are still available (this index is located in the back of the book).

Circle the appropriate update number on the business reply card (centerfold), add postage, and drop it in the mail to receive the complete data sheet of your choice. To order publications without an update number, please use the order number provided in the index and write it in one of the blanks provided on the reply card. Due to the costs of handling and mailing, we ask that you limit your requests to no more than 5 items.

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As integrated circuits become more and more complex, the benefit of consistently high quality products becomes increasingly more important to customers, many of whom have long recognized National as *the* outstanding supplier of top quality products. Such recognition is the result of a management-driven Quality Improvement Program that has pervaded every manufacturing operation, from product design through assembly and packaging at National Semiconductor Corporation. Progress has been nothing less than dramatic, and National's commitment to quality will remain unrelenting in the decades to come.

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February 1983

National Semiconductor

AH5020C Monolithic Analog Current Switch

General Description

A versatile dual monolithic JFET analog switch economically fulfills a wide variety of multiplexing and analog switching applications.

These switches may be driven directly from standard 5V logic.

The monolithic construction guarantees tight resistance match and track.

Features

■ Interfaces with standard TTL	
■ "ON" resistance match	2 ohms
■ Low "ON" resistance	150 ohms
■ Very low leakage	50pA
■ Large analog signal range	±10V peak
■ High switching speed	150ns
■ Excellent isolation between channels	80dB at 1kHz

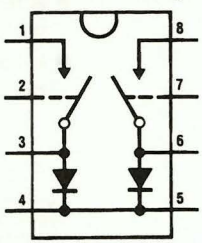
Applications

- AD/DA converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family.

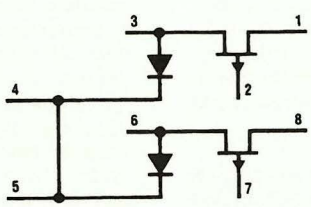
Connection and Schematic Diagrams

Dual-In-Line Package



TOP VIEW

TL/H/5166-1



TL/H/5166-2

Note: All diode cathodes are internally connected to the substrate.

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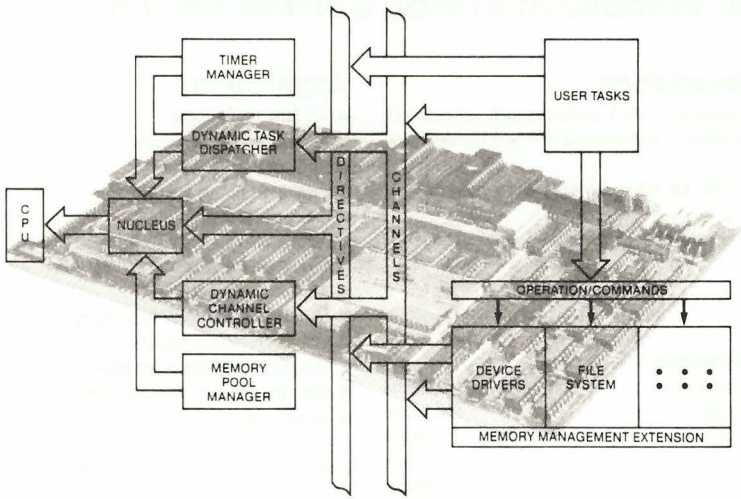
Circle DATA UPDATE No. 101020

National Semiconductor

March 1983

BLMX-16
Board Level Multitasking Executive



- **Provides a multitasking executive for real-time applications**
- **Supports all NS16000 CPUs**
- **Compatible with BLMX-80**
- **Easily Configurable**
  - —Fully user configurable
  - —Hardware independent
- **Extensive user oriented support**
  - —Terminal/printer handlers
  - —Memory pool management
  - —Analog handlers
  - —High-level language interfaces
  - —Disk file system
- **ROMable**
- **Reconfigurable**
- **Real-time clock support for time-of-day and event scheduling**
- **Allows up to 256 levels of task priority which can be dynamically assigned**
- **Incorporates 256 I/O channels for task communication**

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Product Overview

BLMX-16 (Board Level Multitasking Executive for NS16000 CPUs) is National Semiconductor's sophisticated but user friendly real-time multitasking executive for board level computers. Its primary purpose is to simplify the task of designing application software and provides a base upon which users can build a wide range of application systems.

BLMX-16 requires only 2K bytes of RAM and only 4K bytes of ROM and is fully compatible with National Semiconductor's NS16000 CPU family and the DB16000 development board.

BLMX-16 allows the user to monitor and control multiple external events that occur asynchronously in real-time, such as intertask communications, system resource access based upon task priority, real-time clock control, and interrupt handling. These functions greatly simplify application development in such areas as instrumentation and control, test and measurement, and data communications. In these applications, BLMX-16 provides an environment in which system programmers can immediately implement software for their particular application without regard to the details of the system interaction.

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Circle DATA UPDATE No. 101586

National Semiconductor

February 1983

COP410C/COP411C, COP310C/COP311C and COP210C/COP211C Single-Chip CMOS Microcontrollers

General Description

The COP410C, COP411C, COP310C, COP311C, COP210C, and COP211C fully static, single-chip CMOS microcontrollers are members of the COPS™ family, fabricated using double-poly, silicon-gate CMOS technology. These controller-oriented processors are complete microcomputers containing all system timing, internal logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture, and I/O scheme designed to facilitate keyboard input, display output, and BCD data manipulation. The COP411C is identical to the COP410C but with 16 I/O lines instead of 20. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized controller-oriented processor at a low end-product cost.

The COP310C/COP311C is the extended temperature range version of the COP410C/COP411C, and the COP210C/COP211C is the military temperature range version of the COP410C/COP411C.

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Features

- Lowest power dissipation (40 μW typical)
- Low cost
- Power-saving HALT mode with Continue function
- Powerful instruction set
- 512 x 8 ROM, 32 x 4 RAM
- 20 I/O lines (COP410C)
- Two-level subroutine stack
- DC to 4 μs instruction time
- Single supply operation (2.4V to 5.5V)
- General purpose and TRI-STATE® outputs
- Internal binary counter register with MICROWIRE™ compatible serial I/O
- LSTTL/CMOS compatible in and out
- Software/hardware compatible with other members of the COP400 family
- Extended temperature (−40°C to +85°C) devices available
- Military temperature (−55°C to +125°C) devices to be available

Note: At time of printing electrical specifications were not available.

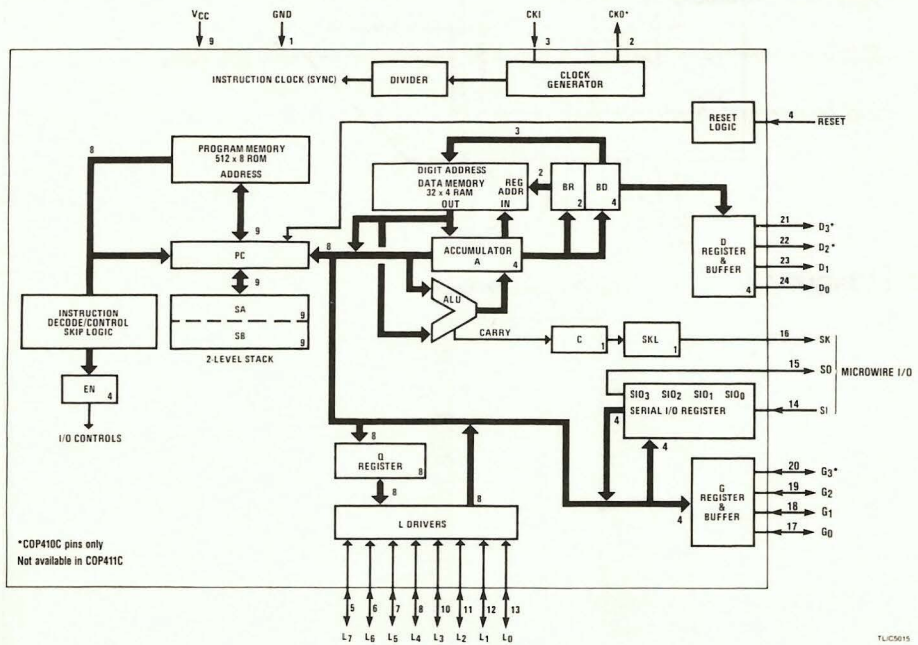

FIGURE 1. COP410C/411C Block Diagram

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Circle DATA UPDATE No. 101965

COP410C/COP411C, COP310C/COP311C and COP210C/COP211C Single-Chip CMOS Microcontrollers

National Semiconductor

April 1983

DAC1266A, DAC1266 Hi-Speed 12-Bit D/A Converter

General Description

The DAC1266A and DAC1266 are fast 12-bit digital to analog converters. These DACs use 12 precision high speed bipolar current steering switches, control amplifier, and a thin film resistor network to obtain a high accuracy, very fast analog output current. The DAC1266A and DAC1266 have 10%–90% full-scale transition time under 30 ns and settle to less than 1/2 LSB in 200 ns.

These digital to analog converters are recommended for applications in CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

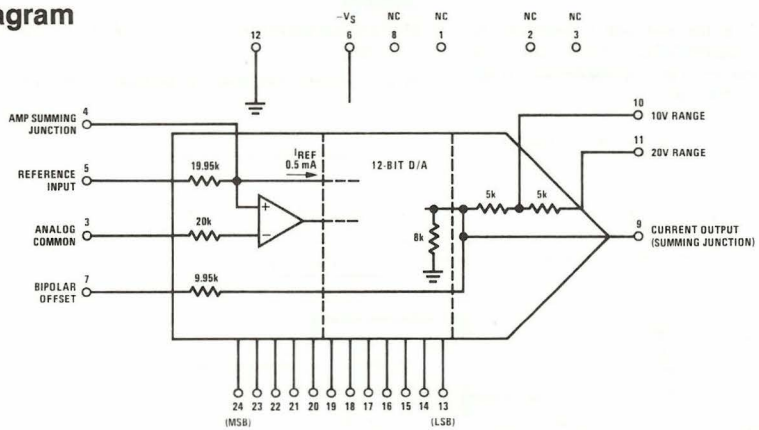
Features

- Bipolar current output DAC
- Fully differential, non-saturating precision current switch — R_{OUT} and C_{OUT} do not change with digital input code
- Precision thin film resistors for use with external op amp for voltage out or as input resistors for a successive approximation A/D converter
- Superior replacement for 12-bit D/A converters of this type

Key Specifications

- Resolution and Monotonicity — 12 Bits
- Linearity (Guaranteed over temperature) — 12 Bits
- Output Current Settling Time — 400 ns max to 0.01%
- Full-Scale Transition Time (10%–90%) — 30 ns
- Power Supply Sensitivity — ± 15 ppm of FS/% V_{SUPPLY}

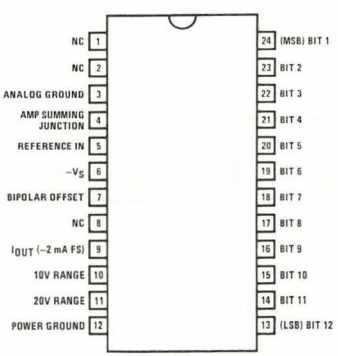
Block Diagram



TL/H/5068-1

Connection Diagram

Dual-In-Line Package



TL/H/5068-2

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Circle DATA UPDATE No. 102400

National Semiconductor

March 1983

DM75S06/DM85S06 Open-Collector DM75S07/DM85S07 TRI-STATE DM75S07A/DM85S07A High Speed TRI-STATE Non-Inverting, 64-Bit (16 × 4) RAMs

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM75S06.

Write Cycle: The information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM85S07 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

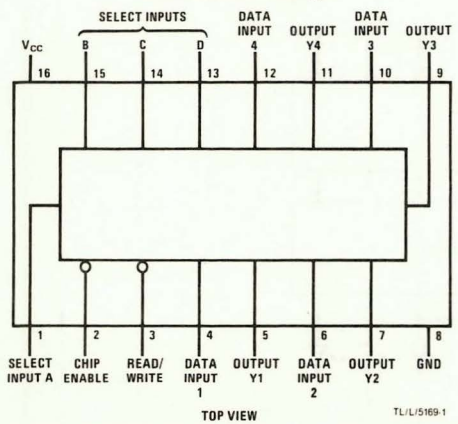
The fast access time of the DM75S07A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM75S07 outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

- Schottky-clamped for high speed applications (75S07A)
  - access from chip-enable input 17 ns max
  - access from address inputs 25 ns max
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM75S06, DM85S06 are functionally equivalent and have open-collector outputs
- DM75SXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL logic circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/L/5169-1

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level
L = Low Level
X = Don't Care

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Circle DATA UPDATE No. 102710

DM75S06/DM85S06 Open-Collector, DM75S07/DM85S07 TRI-STATE® DM75S07A/DM85S07A High Speed TRI-STATE Non-Inverting, 64-Bit (16 × 4) RAMs

National Semiconductor

February 1983

DM77/87SR181
(1024 × 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR181 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on chip. This devices is organized as 1024-words by 8-bits and is available in the tri-state output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR181 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

The DM77SR181 also features an initialize function $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable register INITIALIZE
- 24-pin, 300 mil package
- 40ns address setup and 20ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE® outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

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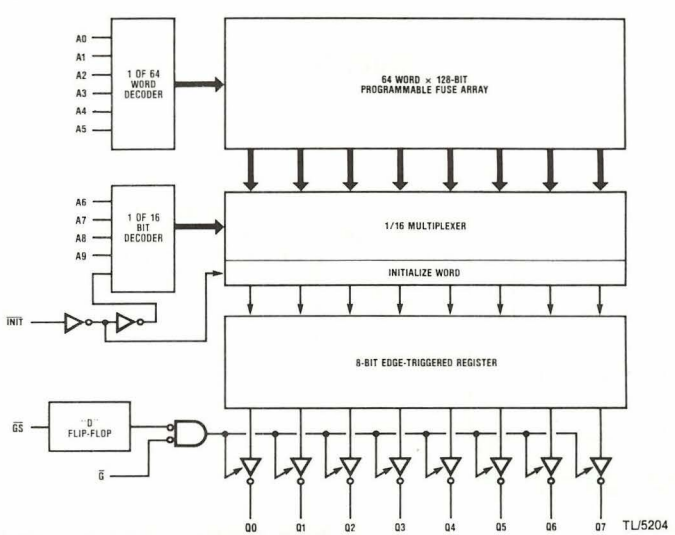
TRI-SAFE™ is a trademark of National Semiconductor Corp.

Block Diagram



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National Semiconductor

PRELIMINARY
February 1983

DM77/87SR474 (512 × 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR474 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR474 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

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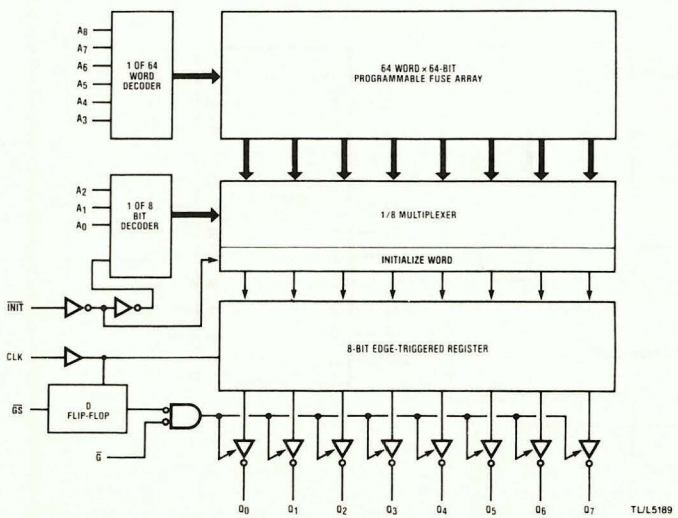
The DM77/87SR474 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows, providing a $\overline{CLEAR}$ function when not programmed.

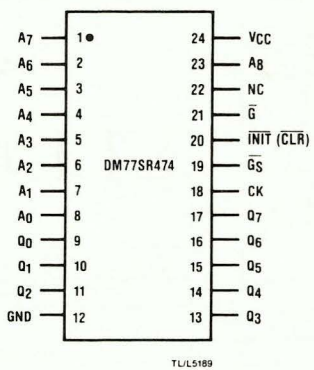
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable synchronous register INITIALIZE
- 24-pin, 300 mil thin-dip package
- 35ns address setup and 20ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature
- Pinout compatible with DM77SR181 (1k × 8) Registered PROM for future expansion

Block and Connection Diagrams





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Circle DATA UPDATE No. 102871

National Semiconductor

PRELIMINARY
February 1983

DM77/87SR476, DM77/87SR25 (512 × 8) 4k-Bit Registered TTL PROM

DM77/87SR476, DM77/87SR25 (512 × 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR476 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR476 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

The DM77SR476 also features an initialize function, $\overline{INIT}$.

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TRI-SAFE™ is a trademark of National Semiconductor Corp.

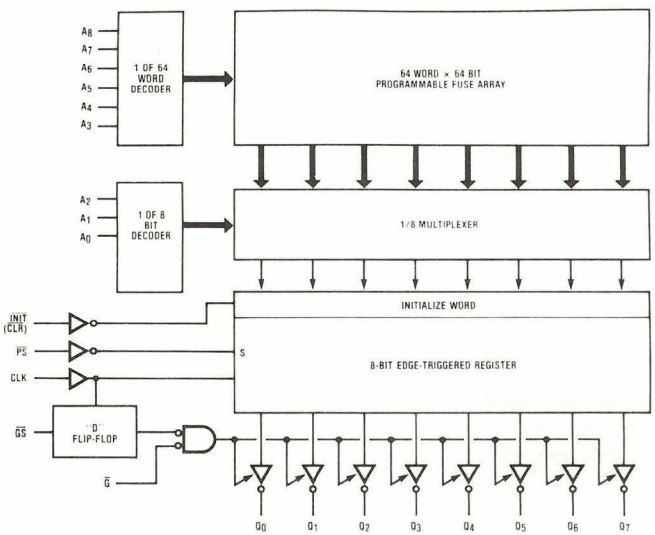
The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows, which makes it compatible with the CLEAR function on the AM27525. $\overline{PS}$ loads ones into the output registers when brought low.

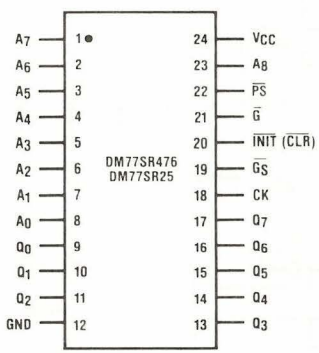
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27525
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable asynchronous INITIALIZE
- 24-pin, 300 mil thin-dip package
- 35ns address setup and 20ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature
- Preset input

Block and Connection Diagrams





TL/L5190

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Circle DATA UPDATE No. 102873

National Semiconductor

PRELIMINARY
February 1983

DM10900 8-Bit Parity ALU Slice

General Description

The DM10900 8-Bit Microprocessor slice is a cascadable device designed for use in high performance central processing units, microprogrammable controllers, and other applications where hardware/software flexibility, ease of expansion, and ECL 10k compatibility are system requirements. The building block architecture and microinstruction format of the DM10900 permits efficient emulation of most digital systems.

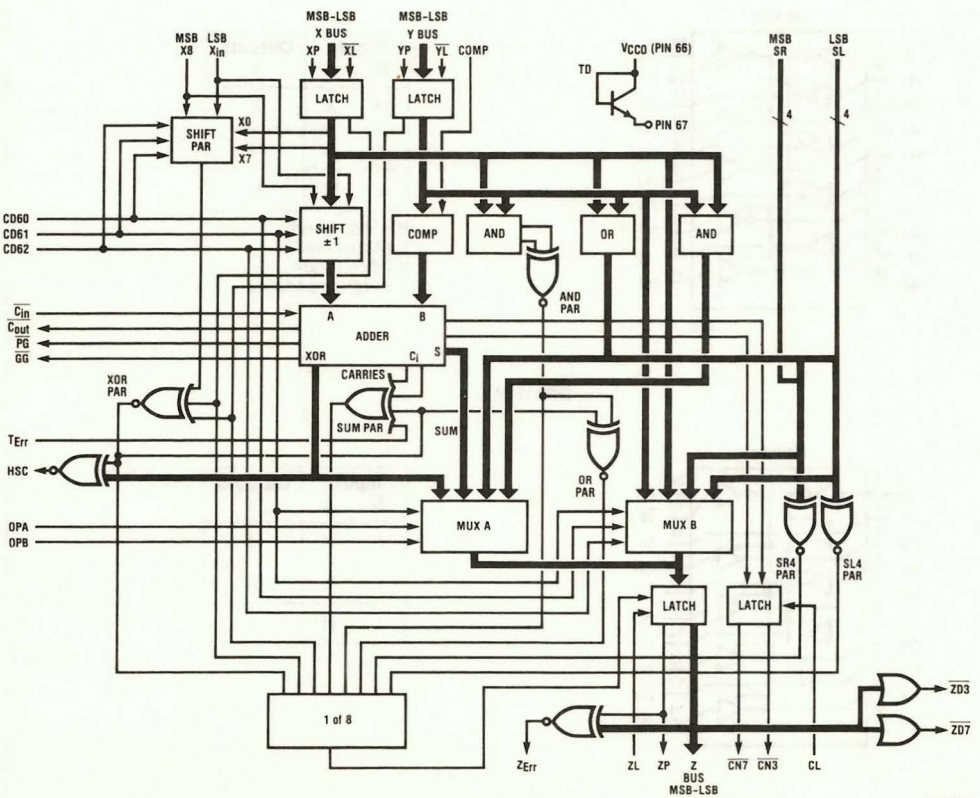
As shown in the block diagram below, the DM10900 consists of a parallel 8-bit adder accessed by two latched input ports. In addition, various logic operations can also be performed on the input data. Shifting circuits and parity detect circuits implemented with ECL, oxide-isolated technology, allow the device to function as a very powerful, high performance ALU.

Features

- Manufactured from high performance, oxide-isolated ECL macrocell array.
- Performs all necessary logic and arithmetic operations.
- Dual port architecture—two 8-bit, latched input ports; one 8-bit, latched output port.
- Internal look-ahead carry with propagate/generate outputs.
- Internal parity detect circuit with parity error output.
- Expandable in 4- or 8-bit increments to form larger word sizes.

Block Diagram

DM10900



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Circle DATA UPDATE No. 102540

National Semiconductor

February 1983

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

General Description

The DP84240 and DP84244 are octal TRI-STATE® drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 250pF and 500pF load capacitances.

Features

- t_{pd} specified with 250pF and 500pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters specified with all outputs switching simultaneously

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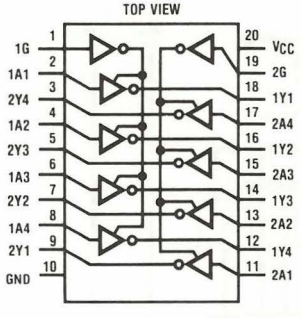
Connection Diagrams

TOP VIEW



TL/F5219

Truth Tables

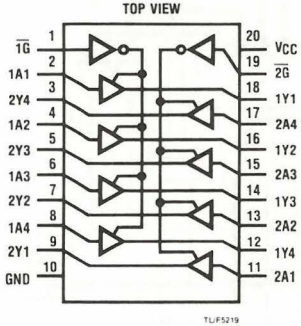
DP84240

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244

TOP VIEW



TL/F5219

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	L
L	H	H

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Circle DATA UPDATE No. 103075

National Semiconductor

March 1983

DS3666 IEEE-488 GPIB Transceiver

General Description

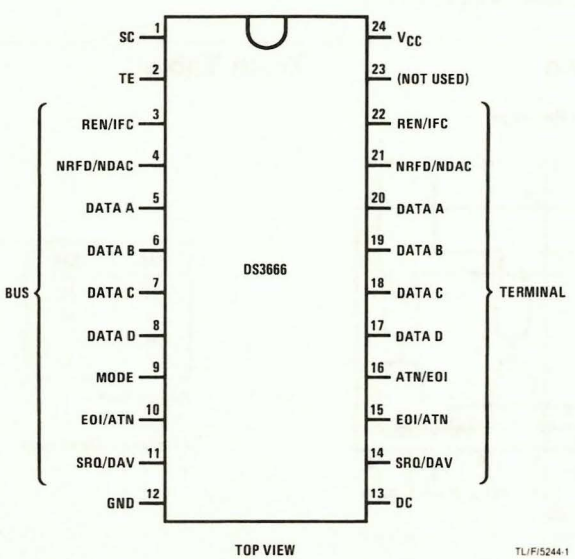
The DS3666 is a high-speed-Schottky 8-channel bi-directional transceiver designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed. A power up/down protection circuit is included at all bus outputs to provide glitch-free operation during V_{CC} power up or down. Implementing the IEEE-488 bus interface is accomplished by connecting two DS3666 devices together using the expansion control inputs provided. Each device is assigned to 4 data channels and 4 management signal channels to achieve the 16-line format.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Power up/down protection (glitch-free)
- Mode control implements 2-device expansion for complete IEEE-488 interface configuration
- Accommodates multi-controller systems

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5244-1

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Circle DATA UPDATE No. 103340

National Semiconductor

PRELIMINARY
March 1983

DS3668 Quad Fault Protected Peripheral Driver

General Description

The DS3668 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. Unlike most peripheral drivers available, a unique fault protection circuit is incorporated on each output. When the load current exceeds 1.0 A (approximately) on any output for more than a built-in delay time, nominally 25 μs, that output will be shut off by its protection circuitry with no effect on other outputs. This condition will prevail until that protection circuitry is reset by toggling the corresponding input or the enable pin low for at least 0.5 μs. The 25 μs built-in delay is provided to ensure that the protection circuitry is not triggered by turn-on surge currents associated with certain kinds of loads.

The DS3668's inputs combine TTL compatibility with high input impedance. In fact, its extreme low input current allows it to be driven directly by a MOS device. The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch up during turn off (inductive fly-back protection — refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3668 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

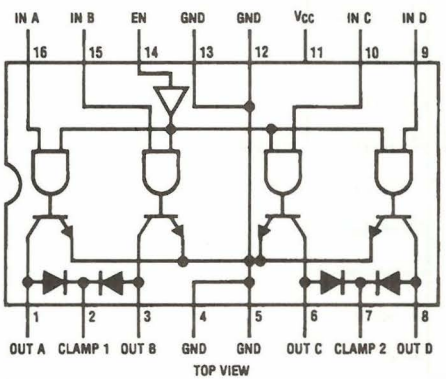
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Output fault protection
- High impedance TTL compatible inputs
- High output current — 600 mA per output
- No output latch-up at 35V
- Low output ON voltage (550 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly-back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail-safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TL/F/5225–1

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

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Circle DATA UPDATE No. 103342

April 1983

National Semiconductor

DT1058 Digitalker™ "EPROMTALKER" Board

General Description

The DT1058 "EPROMTALKER" circuit board is a simple one piece unit which when used with the National Semiconductor MM54104 Speech Processor Chip permits the "playing" of EPROMs containing synthetic speech data. This speech data can be created by the Digitalker Vocabulary Selection System (DVSS) or by the National Semiconductor Speech Laboratory. The MM54104 Speech Processor Chip (SPC) addresses up to 128k bits of speech data directly, without external logic. In Digitalker applications where ROM masking is not feasible, or for applications where systems are prototyped prior to ROM masking, an SPC interface to EPROMs is necessary.

The DT1058 is socketed to hold up to eight 2716 (or 2516) 16k bit EPROMs or four 2732 32k bit EPROMs, for up to 128k bits of synthetic speech storage. The DT1058 includes a decoder IC which performs chip selection for the proper 2716 or 2732 in the vocabulary.

Interface to the DT1058 "EPROMTALKER" is accomplished via a standard 24 pin dip socket.

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Features

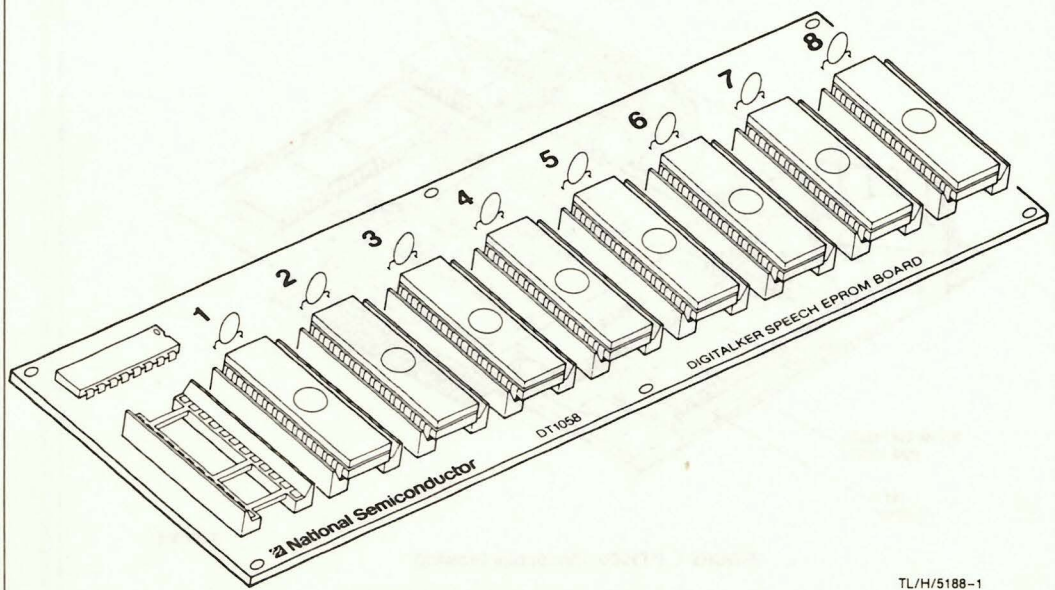
- Accommodates up to 8–2716 or 4-2732 type EPROMs.
- Addresses up to 128k continuous bits of speech data.
- Completely self contained, including chip select decoder.
- Directly interfaces to DT1000 "Digitalker Evaluation Board".
- Supports National Semiconductors Digitalker Vocabulary Selection System DTSW–500.

Applications

Evaluating prototype EPROMs prior to ROM masking speech.

Low volume OEM products utilizing speech EPROMs.

Graphic Overview



TL/H/5188–1

FIGURE 1. DT1058 Conceptual Drawing

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Circle DATA UPDATE No. 104262

March 1983

National Semiconductor

DT1060 "COP™ TALKER" Control ROM

General Description

The DT1060 COP TALKER CONTROL ROM is a 16k Bit ROM designed to allow auditioning of custom generated speech vocabularies through National Semiconductor's DT1000 Digitalker™ Evaluation board and DT1058 "EPROMTALKER" board. National Semiconductor also supplies a DT1058 "EPROMTALKER" board (which accepts up to eight 2716 type speech EPROMS) which can be connected to one of the 24 pin speech ROM sockets on the DT1000 board.

The DT1060 is a special control program interfacing to the COP 402 Microcontroller on the DT1000 board.

When retrofitted into the DT1000, the DT1060 permits independent recall of speech stored at any address in a speech ROM or EPROM set. The DT1060 also provides for repetition or automatic sequencing of speech messages.

This ROM allows quick auditioning of standard ROMs or custom ROMs or EPROMs generated on either National Semiconductors' DTSW–500 Digitalker Vocabulary Selection System or in the National Semiconductor speech lab.

Features

- Simple retrofit into DT1000 Digitalker Evaluation Board
- Allows entry of any address within a Digitalker Speech ROM or EPROM set address.
- Repeats or sequences address automatically

Functional Description

To utilize the DT1060 ROM one should remove the MM52116GZN/N ROM from the lower left hand quadrant of the DT1000 Digitalker evaluation board, and replace it with the DT1060 COP TALKER control ROM.

Make sure that Pin One on the DT1060 corresponds with the Pin "1" mark on the PC Board. The DT1060 socket on the DT1000 board is oriented with Pin One facing the lower or bottom edge of the DT1000 (the same edge connector is located on). See *Figure 1* for a detailed drawing showing the location and orientation of all affected components.

Once the DT1060 has been plugged into the DT1000, the operation is as follows:

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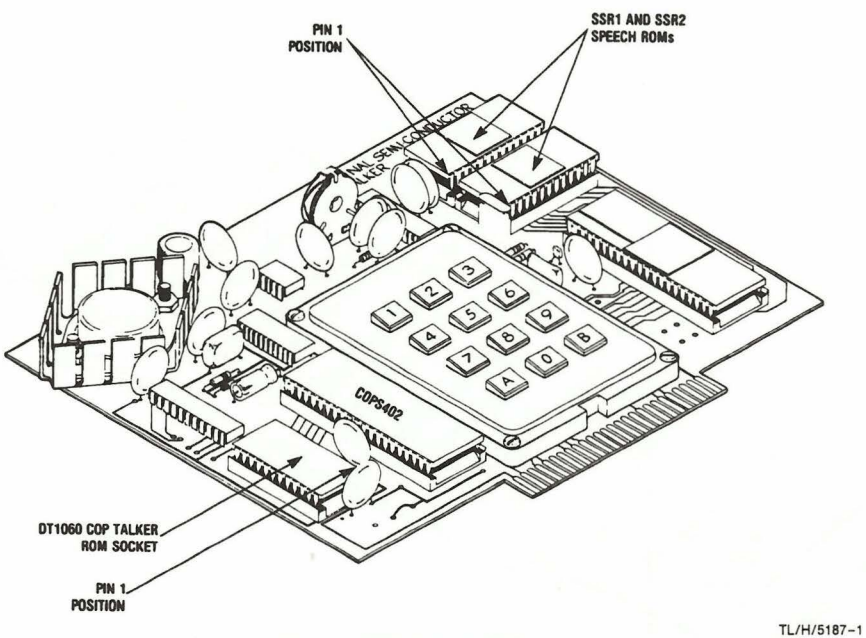
Graphic Overview



TL/H/5187–1

FIGURE 1. DT1000 Conceptual Drawing

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Circle DATA UPDATE No. 104264

National Semiconductor

PRELIMINARY
February 1983

IDM2901A-2 High-Speed 4-Bit Bipolar Microprocessor Slice

General Description

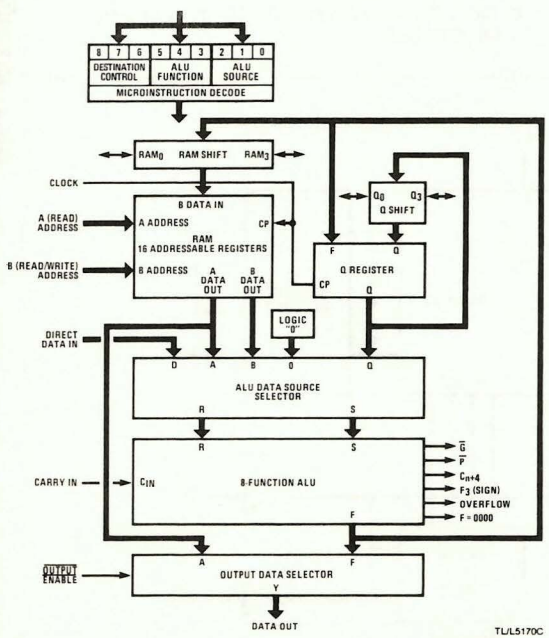
The IDM2901A-2 4-bit bipolar microprocessor slice is a cascadable device designed for use in Central Processing Units, programmable microprocessors, peripheral controllers, and other "high-speed" applications where economy, hardware/software flexibility, and easy expansion are system prerequisites. The building-block architecture and microinstruction format of the IDM2901A-2 permits efficient emulation of most digital-based systems.

As shown in the simplified block diagram, the IDM2901A-2 device consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the required shifting, decoding, and multiplexing circuits. The 9-bit microinstruction word is organized into three groups of three bits each—the first group (bits 0-2) selects ALU source operands, the second group (bits 3-5) selects the ALU function, and the last group (bits 6-8) selects the destination register within the ALU. The slice microprocessor is cascadable with full look-ahead or ripple carry; all outputs are TRI-STATE® and four status-flag outputs are available. To minimize power consumption and to maximize speed and reliability, the 40-pin LSI chip is fabricated using a National state-of-the-art, low-power Schottky technology called "SCL".

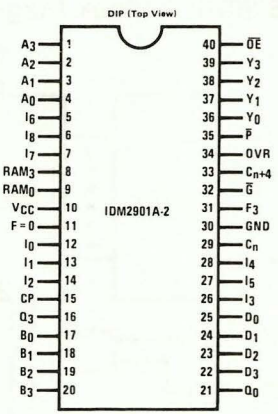
Features and Benefits

- **Multiple-address architecture**—improves system speed by providing simultaneous yet independent access to two working registers.
- **Multifunction ALU**—performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible, data-source selection**—for every ALU function, data is selected from five source ports for a total of 203 source operand pairs.
- **Left/right shift independent of ALU**—an arithmetic operation and a left or right shift can be obtained on the same machine cycle.
- **Four status flags**—carry, overflow, zero, and functional sign are available as outputs.
- **Expandable**—Connect any number of IDM2901A-2s together for longer word lengths.
- **Microprogrammable**—three groups of 3 bits each for source operand, ALU function, and destination control

Block and Connection Diagrams



TL/L5170C



Note: Pin 1 is marked for orientation.

TL/L5170C

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Circle DATA UPDATE No. 104527

IDM2901A-2 High-Speed 4-Bit Bipolar Microprocessor Slice

National Semiconductor

February 1983

IDM29705/29705A 16-Word by 4-Bit Two-Port RAM/Register File

General Description

The IDM29705 and IDM29705A are 16-word by 4-bit RAM/Register File chips housed in a standard 28-pin dual-in-line package. The IDM29705 and the IDM29705A feature TRI-STATE® outputs. These RAMs, which are fabricated using SCL® (Schottky ECL Technology) feature two separate output ports that enable any two 4-bit words to be read from these outputs simultaneously. Each output port contains a four-bit latch. A common Latch Enable (LE) input is used to control all eight latches. The device, which has two Write Enable (WE) inputs, is designed so that either Write Enable ($WE_{1\ or\ 2}$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge-triggered.

The device, which has fully decoded A-address and B-address fields, can address any of the 16 memory words for the A-output port and, simultaneously, select any of the 16 words for presentation at the B-output port. Incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load the new data into the device.

Several of these devices can be cascaded to increase the total number of memory words in the system. When $\overline{OE}$-A is high, the A-output port is in the high-impedance mode. $\overline{OE}$-B, when high, forces the B-output port to the high-impedance state.

The writing of new data into the RAM is controlled by the Write Enable inputs. With both Write Enable inputs low, data is written into the word selected by the B-address field. The memory outputs follow the data inputs during writing if the Latch Enable (LE) is high. With either Write Enable high, no data is written into the RAM.

Features and Benefits

- 16-Word by 4-Bit, 2-Port RAM/Register Files
- Two Output Ports, Each with Separate Output Control
- 4-Bit Latches on Each Output Port
- Non-Inverted Data Output with Respect to Data Input
- Output Enable and Write Enable Inputs Provide Ease in Cascading
- SCL Technology (Schottky ECL) Provides ECL Speeds While Keeping Low Power Schottky Input/Output Voltage and Power Consumption Compatibility
- 100% Reliability Testing in Compliance with MIL-STD-883

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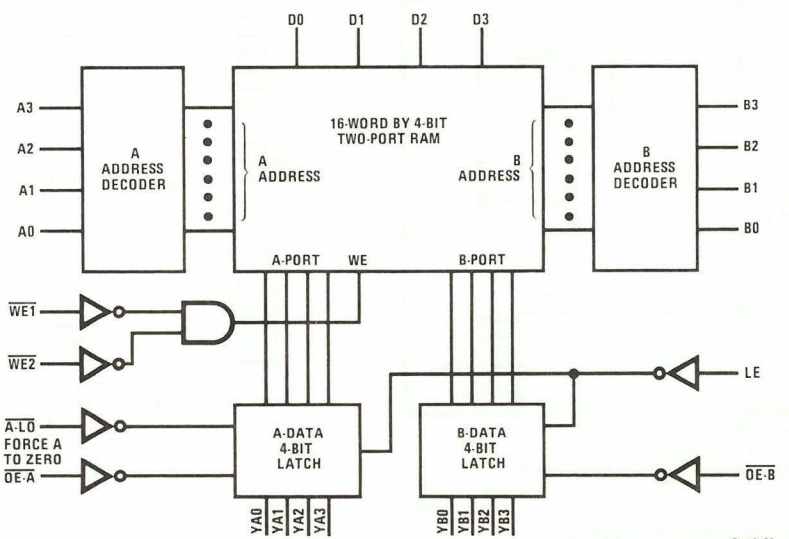
IDM29705/29705A Block Diagram



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Circle DATA UPDATE No. 104602

National Semiconductor

PRELIMINARY
April 1983

LM1036 Dual DC Operated Tone/Volume/Balance Circuit

General Description

The LM1036 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

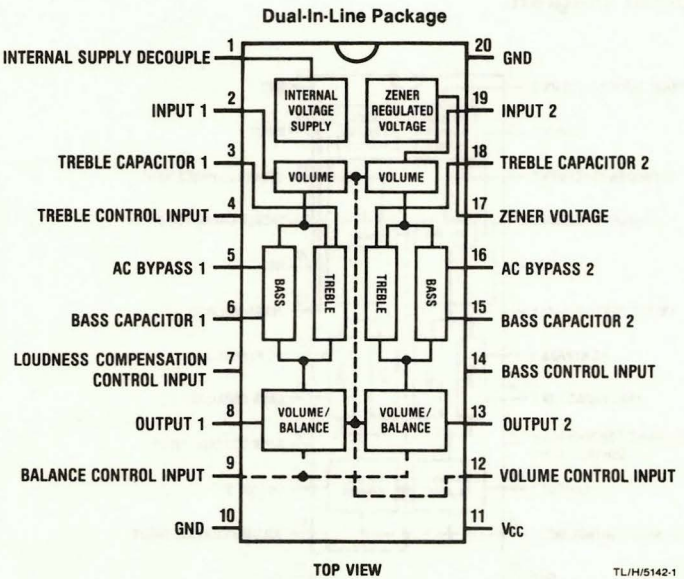
Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ± 15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagram



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Circle DATA UPDATE No. 107296

National Semiconductor

PRELIMINARY
April 1983

LM1040 Dual DC Operated Tone/Volume/Balance Circuit with Stereo Enhancement Facility

General Description

The LM1040 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. A stereo enhancement facility is included whereby the apparent stereo separation of systems requiring closely spaced speakers may be improved. An additional control input allows loudness compensation to be simply effected.

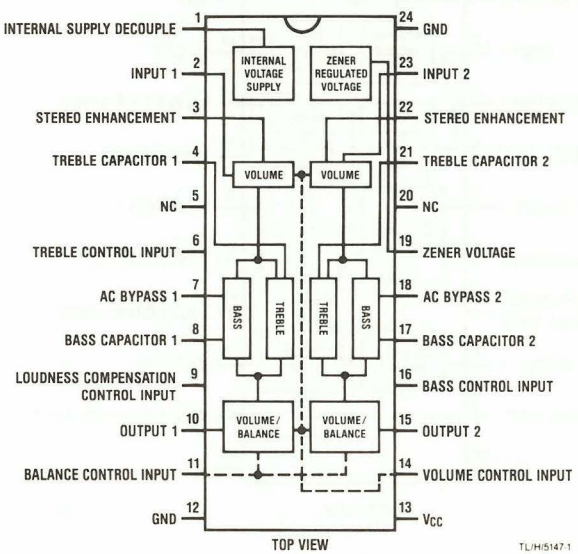
Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ± 15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagram



TOP VIEW

TL/H/5147-1

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Circle DATA UPDATE No. 107298

LM1040 Dual DC Operated Tone/Volume/Balance Circuit with Stereo Enhancement Facility

Takes the mystery out of IC devices and how they work . . .

Never before has there been such a clear and simple explanation of the basic physical actions that take place within solid-state integrated circuits. With this handy guide, you'll be able to easily understand and "feel" the workings of all the devices used in the new semiconductor products—and make better use of them—from the many types of diodes to the bipolar transistors . . . the JFETs . . .the MOSFETs . . . and more.

INTUITIVE IC ELECTRONICS: A Sophisticated Primer for Engineers and Technicians

021923-0 *Thomas M. Frederiksen* 183 pages, $19.95

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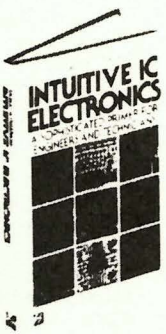

Takes the mystery out of IC devices and how they work . . .

Never before has there been such a clear and simple explanation of the basic physical actions that take place within solid-state integrated circuits. With this handy guide, you'll be able to easily understand and "feel" the workings of all the devices used in the new semiconductor products—and make better use of them—from the many types of diodes to the bipolar transistors . . . the JFETs . . .the MOSFETs . . . and more.

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National Semiconductor

PRELIMINARY
March 1983

LM2935 Low Dropout Dual Regulator

General Description

The LM2935 positive voltage regulator features a low quiescent current of 3 mA or less when supplying 10 mA loads from the standby regulator output. This unique characteristic and the extremely low input-output differential required for proper regulation (0.55V for output currents of 10 mA) make the LM2935 the ideal regulator for power systems that include standby memory. Applications include processor power supplies demanding as much as 750 mA of output current.

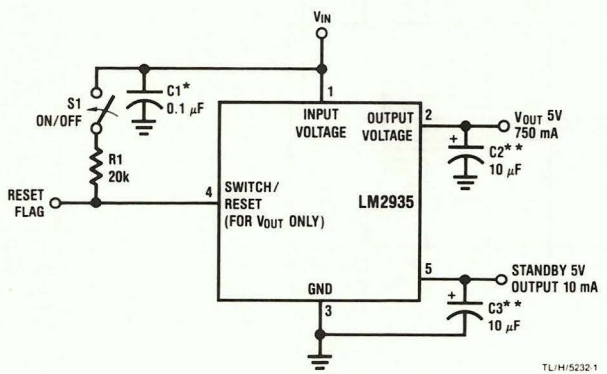
Designed primarily for automotive applications, the LM2935 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load while the standby regulator will continue to power any standby load. The LM2935 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed outputs of 5V are available in the plastic TO-220 power package.

Features

- Two regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in plastic TO-220
- ON/OFF switch for high current output
- Reset error flag
- 100% electrical burn-in

Typical Application Circuit



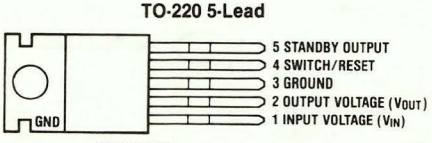
* Required if regulator is located far from power supply filter.

** Required for stability. May be increased without bound. Capacitor must be rated to operate at the minimum temperature expected for the regulator system.

FIGURE 1. Test and Application Circuit

Connection Diagram

TO-220 5-Lead



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Circle DATA UPDATE No. 108015

National Semiconductor

PRELIMINARY
February 1983

MM54HC30/MM74HC30 8-Input NAND Gate

General Description

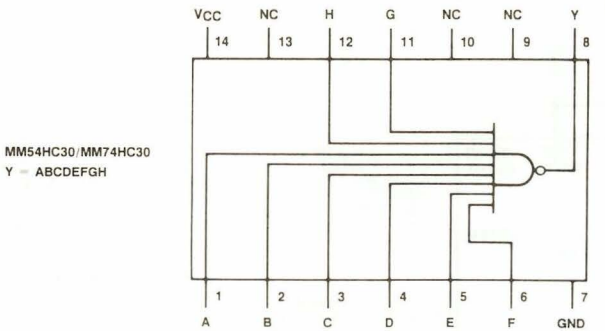
These logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads (8 LSTTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

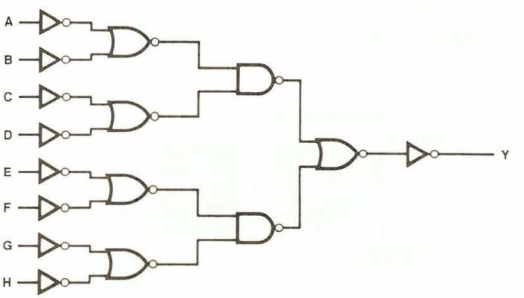
- Typical propagation delay: 20ns
- Wide power supply range: 2-6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

MM54HC30/MM74HC30
(Dual-In-Line Package)



Logic Diagram



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Circle DATA UPDATE No. 111537

National Semiconductor

PRELIMINARY
February 1983

MM54HC133/MM74HC133 13-Input NAND Gate

General Description

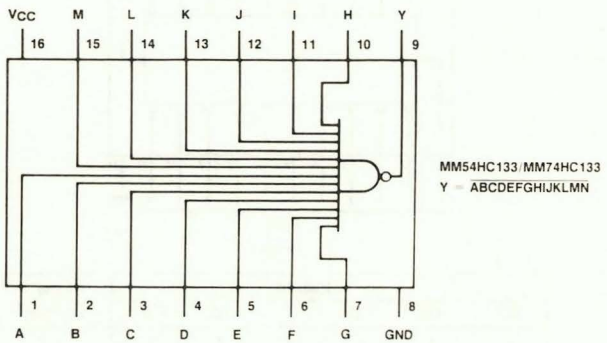
These logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads (8 LSTTL loads for 54HC). The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

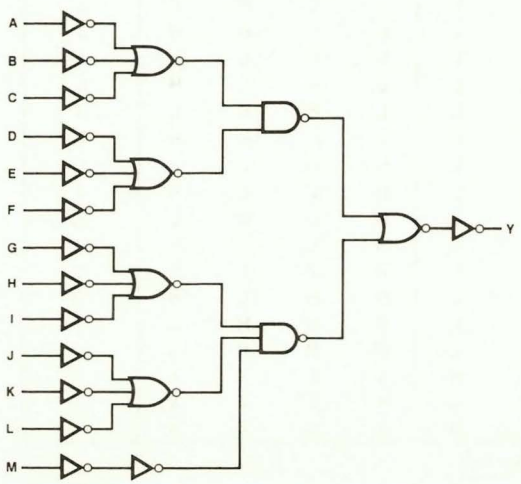
- Typical propagation delay: 20ns
- Wide power supply range: 2-6V
- Low quiescent current: 20μA maximum (74HC series)
- Low input current: 1μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

MM54HC133/MM74HC133
(Dual-In-Line Package)



Logic Diagram



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Circle DATA UPDATE No. 111562

National Semiconductor

PRELIMINARY
April 1983

MM54HC154/MM74HC154 4-to-16 Line Decoder

General Description

This device is a high speed silicon gate CMOS decoder, and is well suited to memory address decoding or data routing applications. It possesses high noise immunity, and low power consumption of CMOS with speeds similar to low power Schottky TTL circuits.

The MM54HC154/MM74HC154 have 4 binary select inputs (A, B, C, and D). If the device is enabled these inputs determine which one of the 16 normally high outputs will go low. Two active low enables ($\overline{G1}$ and $\overline{G2}$) are provided to ease cascading of decoders with little or no external logic.

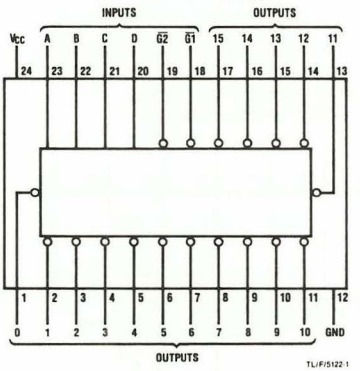
Each output can drive 10 low power Schottky TTL equivalent loads, and is functionally and pin equivalent to the 54LS154/74LS154. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 21 ns
- Power supply quiescent current: 80 μA (74HC)
- Wide power supply voltage range: 2V–6V
- Low input current: 1 μA max

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

Inputs						Low Output*
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

*All others high

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Circle DATA UPDATE No. 111564

National Semiconductor

PRELIMINARY
April 1983

MM54HC245/MM74HC245 Octal TRI-STATE® Transceiver
MM54HC640/MM74HC640 Inverting Octal TRI-STATE Transceiver
MM54HC643/MM74HC643 True-Inverting Octal TRI-STATE Transceiver

MM54HC245/MM74HC245 Octal TRI-STATE Transceiver
MM54HC640/MM74HC640 Inverting Octal TRI-STATE Transceiver
MM54HC643/MM74HC643 True-Inverting Octal TRI-STATE Transceiver

General Description

These silicon gate CMOS TRI-STATE bi-directional buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

Each device has an active low enable input $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC245/MM74HC245 transfers true data from one bus to the other; the MM54HC640/MM74HC640 transfers inverted data from one bus to other and the MM54HC643/MM74HC643 transfers inverted data from the A bus to the B bus and true data from the B bus to the A bus.

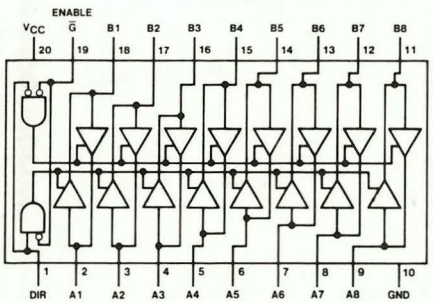
All three devices can drive up to 15 LS-TTL Loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

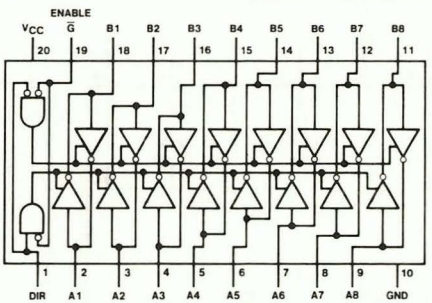
- Typical propagation delay: 14ns
- Wide power supply range: 2-6V
- Low quiescent supply current: 80μA maximum (74 HC)
- Tri-State outputs for connection to bus oriented systems
- High Output Drive: 6mA (min)

Connection Diagrams

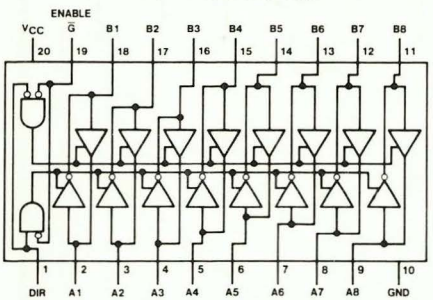
MM54HC245/MM74HC245
Dual-In-Line Package



MM54HC640/MM74HC640
Dual-In-Line Package



MM54HC643/MM74HC643
Dual-In-Line Package



Truth Table

Control Inputs		Operation		
$\overline{G}$	DIR	245	640	643
L	L	B data to A bus	$\overline{B}$ data to A bus	B data to A bus
L	H	A data to B bus	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

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Circle DATA UPDATE No. 111619

National Semiconductor

PRELIMINARY
April 1983

MM54HC4049/MM74HC4049 Hex Inverting Logic Level Down Converter
MM54HC4050/MM74HC4050 Hex Logic Level Down Converter

General Description

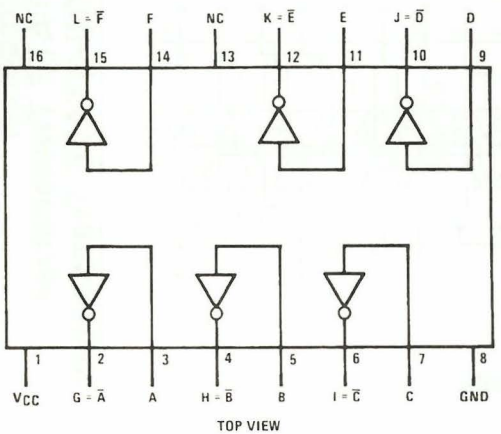
The MM54HC4049/MM74HC4049 and the MM54HC4050/MM74HC4050 have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low level logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC} thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a simple buffer or inverter without level translation. These devices are implemented in silicon gate CMOS. The MM54HC4049/MM74HC4049 is pin and functionally compatible to the CD4049BM/CD4049BC and the MM54HC4050/MM74HC4050 is compatible to the CD4050BM/CD4050BC.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 20 μA max (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagrams

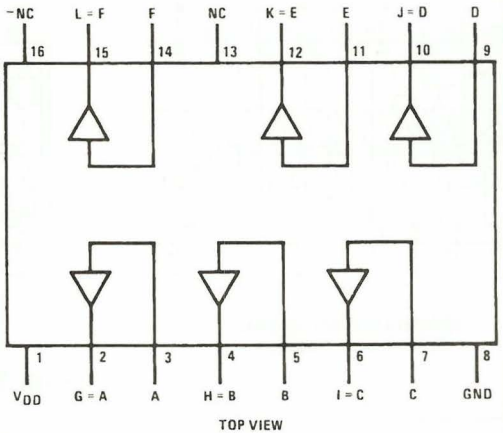
MM54HC4049/MM74HC4049
Dual-In-Line Package



TOP VIEW

TL/F/5214–1

MM54HC4050/MM74HC4050
Dual-In-Line Package



TOP VIEW

TL/F/5214–2

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National Semiconductor

PRELIMINARY
March 1983

MM57409 Super Number Cruncher

General Description

The Super Number Cruncher (SNC) is an MOS/LSI arithmetic processor (actually, a pre-programmed member of National's single-chip microcontroller COPS™ family) intended for use in number processing applications. Scientific calculator functions, conditional output capability, internal number storage, and input/output instructions have been combined in this single chip device. Programming is done in calculator keyboard level language which simplifies software development. Data or instructions can be synchronous or asynchronous, I/O digit count, I/O notation mode, and error control are user programmable; a sense input and flag outputs are available for single bit control; and instructions and lines are available for I/O expansion.

Applications

- Instruments
- Microprocessor/minicomputer peripheral
- Test equipment
- Process controllers

Features

- Scientific calculator instructions (RPN)
  - Up to 12-digit mantissa, 2-digit exponent
  - 4-register stack, one memory register
  - Trigonometric functions, logarithmic functions, Y^x, e^x, π
  - Error flag generation and recovery
- Flexible input/output
  - Multidigit OUT instruction with floating-point or scientific notations
  - Programmable mantissa digit count for OUT instruction
  - Sense input and flag outputs
  - Eight high-impedance I/O lines (TRI-STATE®), six I/O lines, and four output lines for I/O expansion.
- Interface simplicity
  - On-chip clock OSC
  - Generates all I/O control signals
  - MICROBUS™ interface

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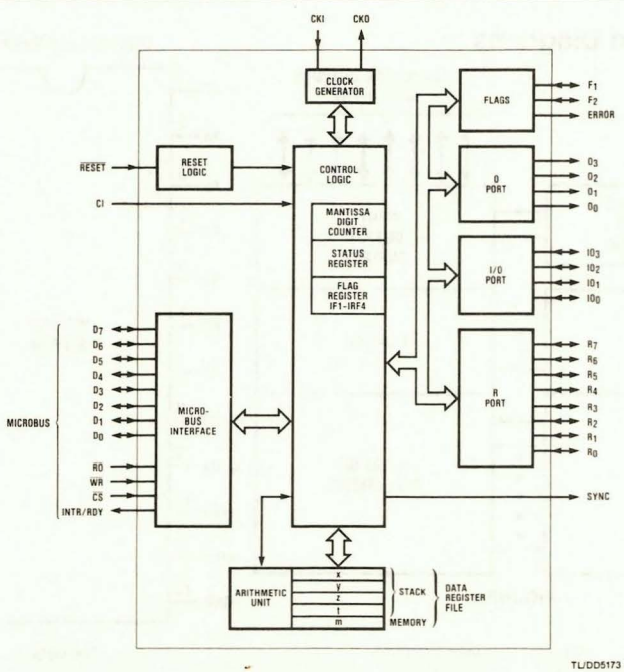

FIGURE 1. SNC Block Diagram

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Circle DATA UPDATE No. 111140

National Semiconductor

PRELIMINARY
April 1982

NMC2816 16k (2k × 8) Electrically Erasable PROM

Max Access/Current	NMC2816-25	NMC2816-35	NMC2816-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC2816 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816 is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC2816 also has an output enable control to eliminate bus contention in a system environment.

The NMC2816 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 × 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816-25)
  - 350 ns max (NMC2816-35)
  - 450 ns max (NMC2816-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 610 mW max (active power ICC + IPP)
  - 295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

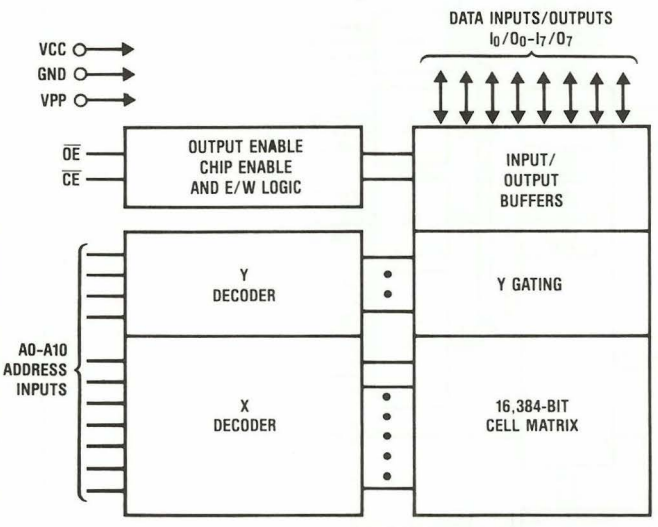
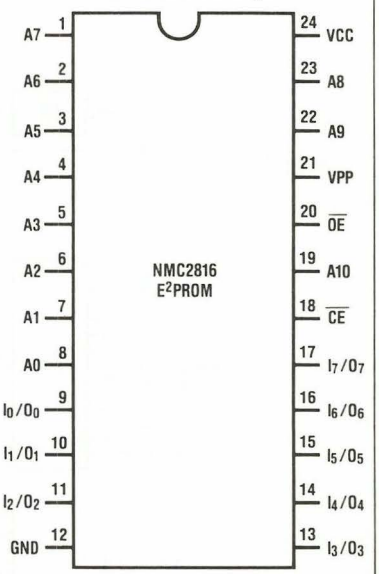


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package



TOP VIEW

FIGURE 2

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Circle DATA UPDATE No. 112234

National Semiconductor

PRELIMINARY
April 1982

NMC2816M 16k (2k × 8) Electrically Erasable PROM

Max Access/Current	NMC2816M-25	NMC2816M-35	NMC2816M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC2816M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816M is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC2816M also has an output enable control to eliminate bus contention in a system environment.

The NMC2816M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 × 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816M-25)
  - 350 ns max (NMC2816M-35)
  - 450 ns max (NMC2816M-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 800 mW max (active power ICC + IPP)
  - 360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

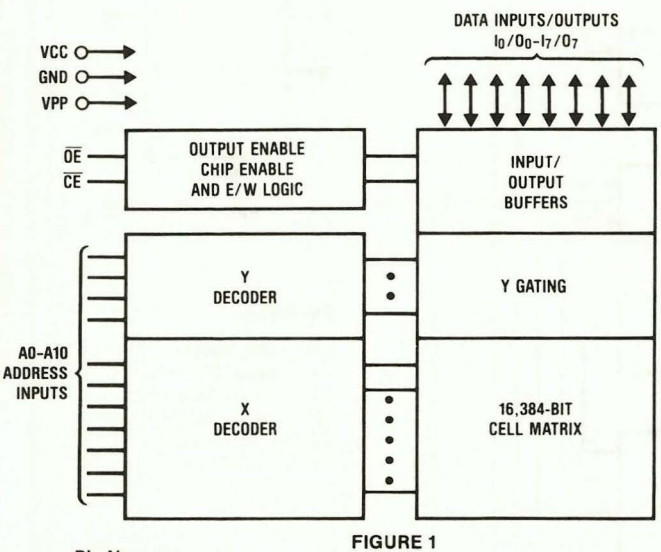
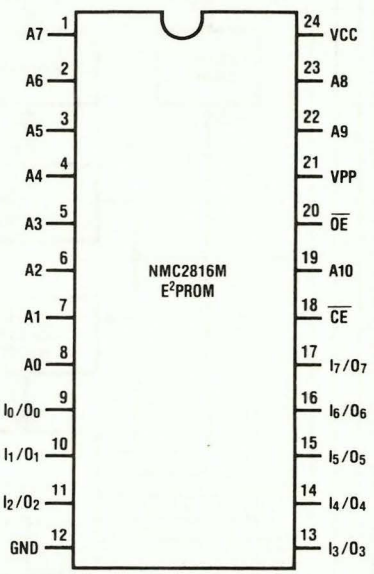


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package



TOP VIEW

FIGURE 2

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Circle DATA UPDATE No. 112262

National Semiconductor

February 1983

NMC9306/COP494 256-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC9306/COP494 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306/COP494 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams

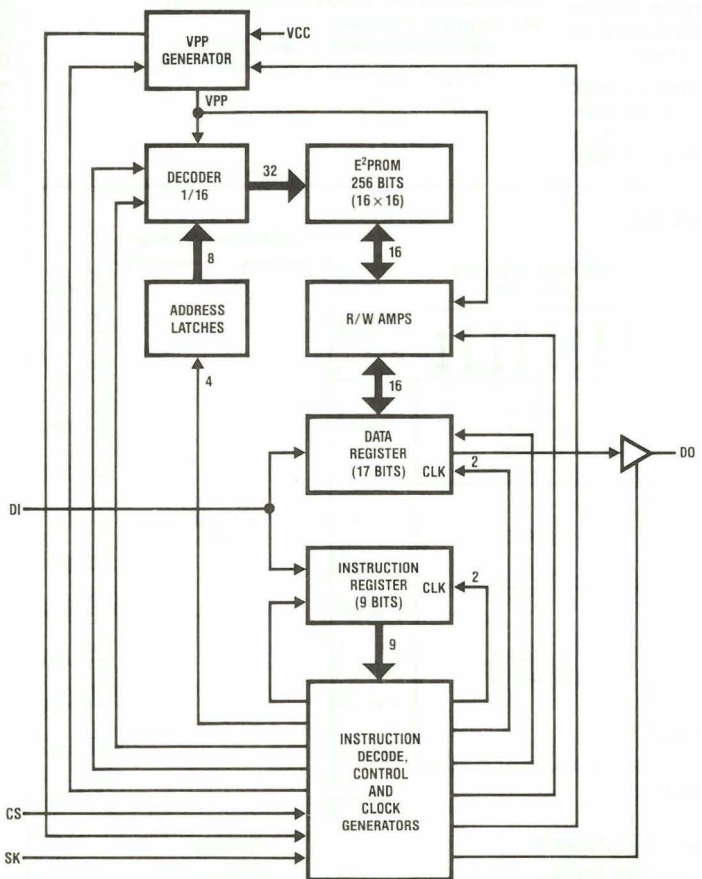

FIGURE 1

Dual-In-Line Package

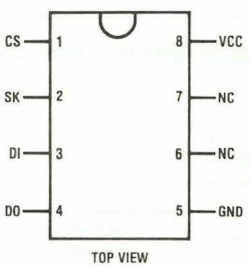

FIGURE 2

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

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Circle DATA UPDATE No. 112270

National Semiconductor

February 1983

NMC9306E/COP494E 256-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC9306E/COP494E is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306E/COP494E has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams

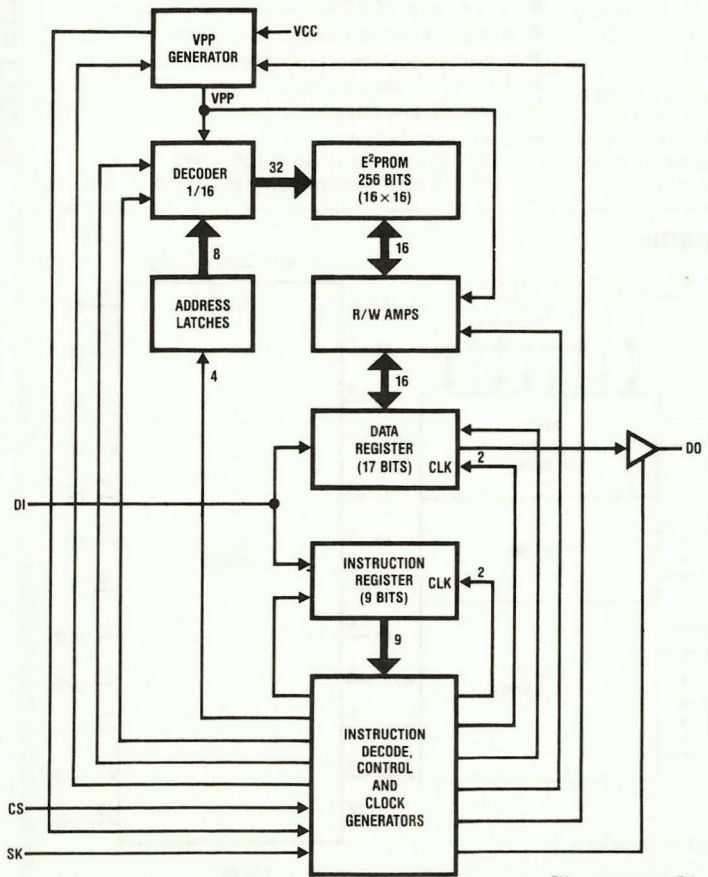

FIGURE 1

Dual-In-Line Package

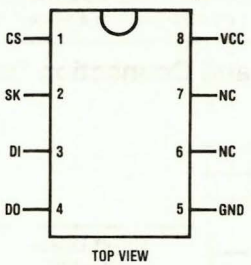

FIGURE 2

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

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Circle DATA UPDATE No. 112272

National Semiconductor

February 1983

NMC9716 16k (2k × 8) Electrically Erasable PROM

Max Access/Current	NMC9716-25	NMC9716-35	NMC9716-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC9716 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716 is pin and functionally compatible with the NMC2816 E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9716 is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC9716 also has an output enable control to eliminate bus contention in a system environment.

The NMC9716 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816
- No rise time restriction on erase/write pulse
- 2048 × 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  610 mW max (active power ICC + IPP)
  295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

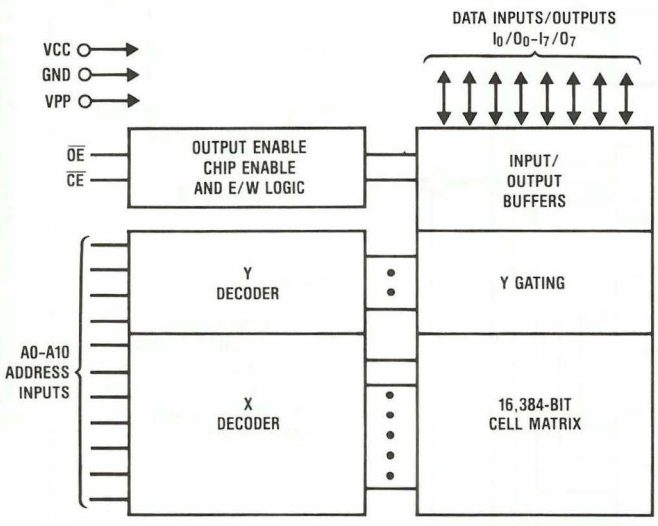
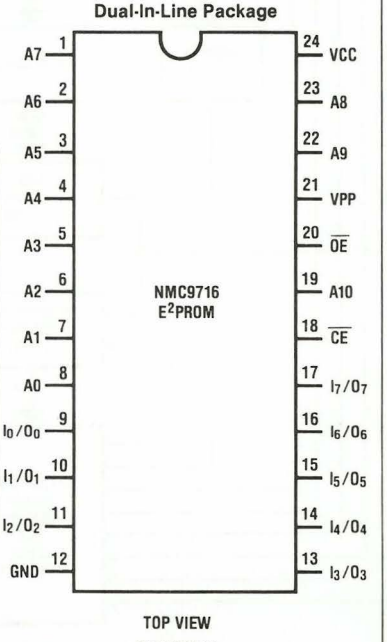


FIGURE 1



TOP VIEW

FIGURE 2

Pin Names

A0–A10	Addresses	O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0–I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

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Circle DATA UPDATE No. 112285

National Semiconductor

February 1983

NMC9716M 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716M-25	NMC9716M-35	NMC9716M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC9716M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716M is pin and functionally compatible with the NMC2816M E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

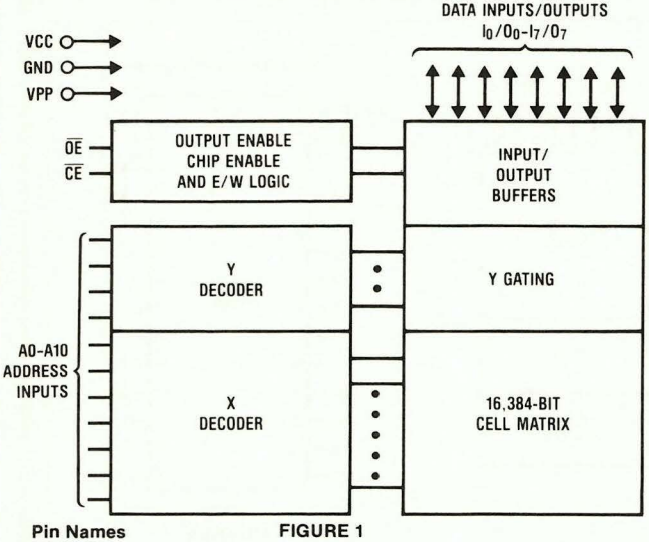
The NMC9716M is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC9716M also has an output enable control to eliminate bus contention in a system environment.

The NMC9716M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816M
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  800 mW max (active power ICC + IPP)
  360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

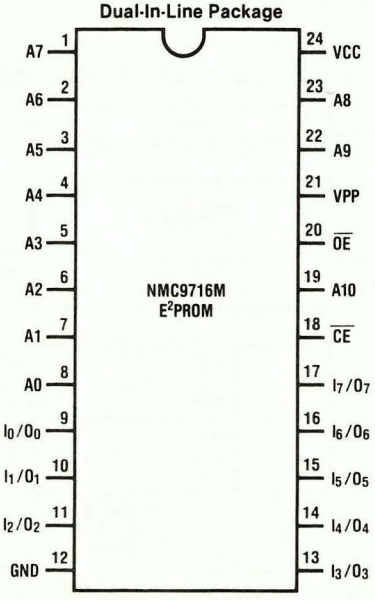


Pin Names

A0–A10	Addresses	O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0–I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

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Circle DATA UPDATE No. 112286

National Semiconductor

PRELIMINARY
April 1983

NMC9817 16,384-Bit (2k × 8) E²PROM

NMC9817 16,384-Bit (2k × 8) E²PROM

General Description

The NMC9817 is a fast 5V-only E²PROM which offers many desired application features, making it ideally suited for efficiency and ease in system design. The added features on the NMC9817 include: 5V-only operation provided by on-chip VPP generation during erase-write; address and data latches to reduce part count and to free the microprocessor while the chip is busy during erase-write; 'ready' line indicator to indicate status of chip to the microprocessor; automatic erase before byte-write; and chip-erase, allowing byte-writes to occur in half the regular erase-write cycle. It can perform up to 10^4 write cycles per byte. The NMC9817 is a product of advanced E²PROM technology and uses the powerful XMOS process for reliable, non-volatile data storage.

The NMC9817 sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the NMC9817 signals 'ready'. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip latching further enhances system performance.

The NMC9817's very fast read access times make it compatible with high performance microprocessor applications. It uses proven two line control architecture which eliminates bus contention in a system environment. Combining these features with the NMC9817's 'ready' signal makes the device an extremely powerful, yet simple to use, E² memory.

The density, and level of integrated control, make the NMC9817 suitable for users requiring no hardware overhead, high system performance, minimal board space and design ease. Designing with and using the NMC9817 is extremely cost effective as the required high voltage and interfacing hardware required for other E²PROM devices has been eliminated by 5V-only operation and on-chip latches. See *Figures 1, 2, and 3* for the NMC9817 block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply (eliminates external 21V VPP)
- Self-timed byte-write with auto erase
- Chip-erase mode for significantly fast E/W cycles
- No external capacitor or pulse shaping circuits
- On-chip address and data latches
- Two line output control
- TRI-STATE® outputs
- RDY pin indicator
- Fast byte-writing
  - Write cycle (5 ms typical)
  - E/W cycle (10 ms typical)
- Very fast access times
  - NMC9817J-20—200 ns
  - NMC9817J-25—250 ns
  - NMC9817J-35—350 ns
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams

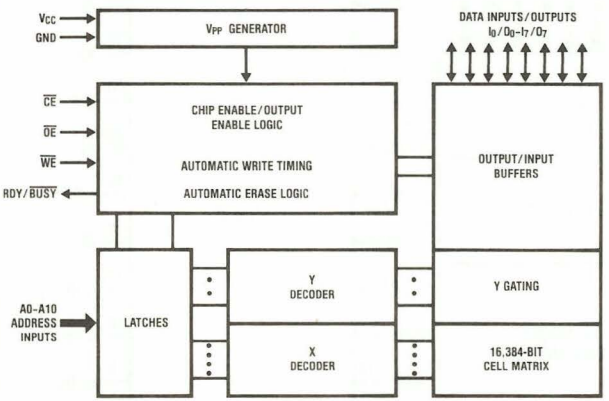
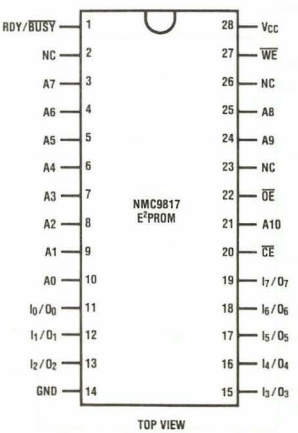


FIGURE 1

Pin Names

A0–A10	Addresses	I_0–I_7	Data Inputs
$\overline{CE}$	Chip Enable	RDY/$\overline{BUSY}$	Device Ready/Busy
$\overline{OE}$	Output Enable	NC	No Connect
O_0–O_7	Data Outputs		

Dual-In-Line Package



TOP VIEW

FIGURE 2

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Circle DATA UPDATE No. 112287

March 1983

National Semiconductor

NMH2864 64k (8k x 8) Electrically Erasable PROM

General Description

The NMH2864 is a 65,536-bit electrically erasable and programmable read-only memory (E^2PROM) incorporating National's high speed, low power, N-channel double silicon gate technology. The device is fabricated by assembling National's NMC2816 16,384 bit (2k x 8) E^2PROM in a hermetic leadless chip carrier (LCC). Three of these LCCs, plus another LCC containing a DM54LS138 control chip along with the NMC2816, are fully screened. All four are then attached to a 28 pin ceramic motherboard in an 8k x 8-bit matrix. The electrical erase/write capability of the NMC2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write. (The density provided by the NMH2864 configuration makes it ideal for those applications where board space is limited, yet high memory density is essential, such as airborne computers.)

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors such as the NS16032.

The NMH2864 is automatically placed in the standby mode and de-selected when the $\overline{CE}$ input is high. This mode provides a 50% reduction in power with no increase in access time. To eliminate bus contention in a system environment, the NMH2864 also has an output enable control.

The NMH2864 can be easily erased and reprogrammed in a byte-by-byte mode. In addition, each of the four memory arrays can be bulk erased independently with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic ones (TTL high).

Features

- Reliable floating gate technology
- High density innovative packaging
- 8k x 8 organization
- Intended to be pin compatible with proposed monolithic devices
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  - 1,130 mW max (active power ICC + IPP)
  - 470 mW max (standby power ICC + IPP)
- Fast access time — 450 ns max
- Available with MIL-STD-883, Class B screening of individual LCC packages

Block and Connection Diagrams

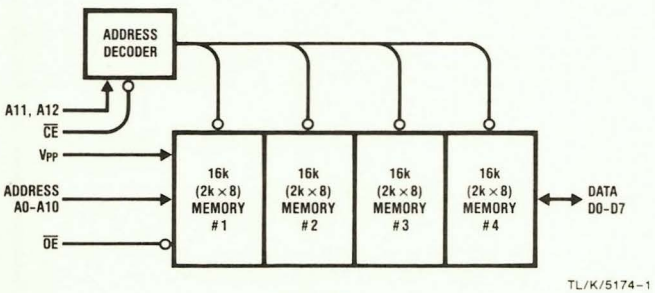

FIGURE 1.

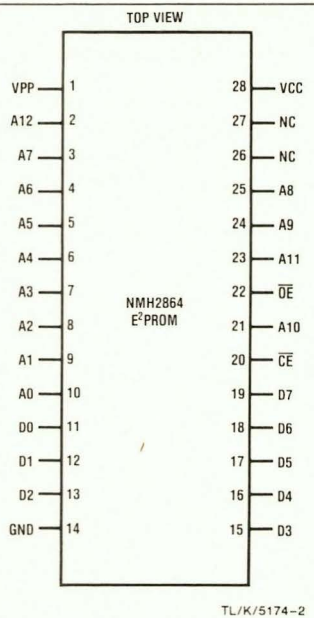

FIGURE 2.

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Circle DATA UPDATE No. 112288

THE DATA BOOKSHELF: TOOLS FOR THE DESIGN ENGINEER

National Semiconductor's Data Bookshelf is a compendium of information about a product line unmatched in its breadth in the industry. The eleven independent volumes that comprise the Bookshelf—about 6000 pages—describe in excess of 8100 solid-state devices; devices that span the entire spectrum of semiconductor processes, and that range from the simplest of discrete transistors to microprocessors—those most-sophisticated marvels of modern integrated-circuit technology.

Active and passive devices and circuits; hybrid and monolithic structures; discrete and integrated components ... complete electrical and mechanical specifications; charts, graphs, and tables; test circuits and waveforms; design and application information...whatever you need, you'll find it in the designer's ultimate reference source—National Semiconductor's Data Bookshelf.

ADVANCED SCHOTTKY DATABOOK

The DM54/74AS family of devices is designed to meet the needs of system designers who require the ultimate in speed. AS achieves the fastest prop delays bipolar technology can offer (2 ns per gate). The AS family also offers significant reduction in power dissipation (8 mW per gate) over present Schottky (54/74S) with toggle rate capability of up to 200 MHz.

The AS family is TTL pinout compatible and offers Schottky (54/74S) drive capability with better fanout, higher noise immunity and faster operation.

For maximum design flexibility and elimination of special drawings, the AS family will be introduced with $\pm 10\%$ V_{CC} over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and V_{CC} range.

Page Count: 172 Price: $5.00 Year: 1982

AUDIO/RADIO HANDBOOK

This 240-page handbook acquaints those involved in audio systems design with National Semiconductor's broad selection of integrated circuits specifically designed for accurate audio reproduction.

Far from just a collection of data sheets, this manual contains detailed discussions including complete design particulars, covering many areas of audio.

Thorough explanations, complete with real-world design examples, make clear several audio areas never before available to the general public.

Page Count: 240 Price: $5.00 Year: 1980

COPS MICROCONTROLLERS DATABOOK

The COPS Microcontrollers Databook offers the most current information available from National Semiconductor on the COPS microcontroller family. Included in this publication are sections on: single-chip, ROMless and piggyback microcontrollers, standard controllers, MICROWIRE peripherals, EPROMs and support circuits, and development systems and user's manuals, as well as the applications for these products.

COPS products offer cost efficiency and design flexibility as well as development ease, and will be continually upgraded and expanded. Continue to look for future databooks providing information on new developments which may improve your capability to bring your ideas to market.

For more information, contact your National Semiconductor Representative concerning any of our COPS family products.

Page Count: 834 Price: $6.00 Year: 1982

48-SERIES MICROCOMPUTER HANDBOOK

This handbook contains detailed design-related information pertaining to the National Semiconductor 48-Series single-chip microcomputers and microprocessors.

The material presented is at a level of detail to aid in the design and development of systems using the 48-Series microcomputers.

Topics include the 48-Series architecture, expansion, and instruction set.

Additional hardware examples, integrated with the required software, and various data sheets of compatible devices are given.

Page Count: 192 Price: $5.00 Year: 1980

HYBRID PRODUCTS DATABOOK

The Hybrid Products Databook is the only National Semiconductor publication that contains complete information on all of our hybrid semiconductor products.

Included are precision thin film and thick film products which provide the user with standard functions from operational amplifiers to converters with capabilities beyond those of current monolithic technology.

Product selection guides and an application section are also included.

Page Count: 792 Price: $7.00 Year: 1982

LINEAR APPLICATIONS HANDBOOK

This 712-page handbook provides a fully indexed and cross referenced collection of 110 linear circuit applications using both monolithic and hybrid circuits from National Semiconductor's broad line of linear products.

Thought provoking applications, written by National's engineers, are an excellent reference source for linear design problems.

Consumer applications, frequency, temperature and drift compensation, and improving signal-to-noise ratios are just a few of the design requirements considered.

Page Count: 712 Price $16.00 Year: 1980

LINEAR DATABOOK

This new 1982 edition of the National Semiconductor Linear Databook is the most comprehensive available. It presents approximately 2000 pages of specifications for our high-technology linear products. Applications, descriptions, features and diagrams in this databook include detailed sections for Voltage Regulators, Op Amps, Voltage Comparators, A to D, D to A Converters, Industrial Blocks and Audio, and TV Circuits.

The databook also features advanced telecommunication devices and speech synthesis (DIGITALKER™), plus other non-state-of-the-art linear products offering performance, economy, quality and reliability.

Page Count: 1952 Price: $12.00 Year: 1982

PAL™ DATABOOK

This book is intended to be a complete reference for the design of digital systems using Programmable Array Logic (PAL) devices. In addition to data sheets for all currently available devices, this book also contains extensive application notes intended to give design examples for a number of PAL devices. It also contains a step-by-step procedure for PAL design and programming, including the listing for PALASM™, which is a FORTRAN IV program that converts logic equations to PAL programming information.

Portions of this book have been reprinted with the permission of Monolithic Memories Inc., the originator of the PAL concept.

Page Count: 176 Price: $6.00 Year: 1982

RELIABILITY HANDBOOK VOLUME I

The Reliability Handbook Volume I penetrates the barrier of technical jargon and procedural ritual that has grown around the subject of semiconductor reliability, enabling the reader to arrive at a clearer understanding in the areas that bear direct concern in the application of semiconductors within the Military/Aerospace electronic systems.

This handbook focuses on areas of concern to all users of semiconductors where device reliability is of paramount importance. It examines the devices themselves and discusses the most widely accepted and specific test procedures designed to test reliability. Throughout, the relationship of electrical, mechanical, environmental, and visual tests and inspections to the nature of the devices is emphasized. Discussions include the MIL-STD-883, MIL-M-38510, VLSI/VHSIC, 883B/RETS™, 883S/RETS™.

The entire book is voluminously documented and comprehensively cross referenced.

Page Count: 285 Price: $7.00 Year: 1982

TRANSISTOR DATABOOK

National Semiconductor has added many new transistors and product families since publication of the last databook. Many have already been widely acclaimed by users.

In addition to small-signal, power-bipolar and field-effect transistors that have been the mainstay of our catalog, there is a section for multiple-field-effect transistors. More part numbers will be added as market needs expand.

To keep current on all new National transistors, please contact your National sales representative or franchised distributor and ask to be placed on the customer mailing list.

Page Count: 558 Price: $6.00 Year: 1982

VOLTAGE REGULATOR HANDBOOK

With the variety of fixed- and variable-regulator technology currently available, the 336-page Voltage Regulator Handbook becomes a must for the selection of three-terminal and dual tracking components that meet the system requirement while utilizing the most cost-effective approach.

Beginning with product selection procedure and a data sheet summary, the text continues with easily accessible information about booster circuitry, power transformer and filter specifications, test methods, manufacturers' cross reference, and extended use applications for National's regulators.

Page Count: 336 Price: $7.00 Year: 1982

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